What is claimed is:

1. A semiconductor integrated circuit having one or more functional circuit blocks and executing a set of instructions, comprising:

a clock supply circuit that supplies one or more clocks for driving said one or more functional circuit blocks at a different frequency; and

a clock selector circuit that selects a clock being fed to each of the functional circuit blocks for each execution cycle,

wherein the clock supply circuit and the clock selector circuit are configured so as to change an operating frequency or halt operation of said one or more functional circuit blocks for each execution cycle.

2. A semiconductor integrated circuit having one or more functional circuit blocks and executing a set of instructions, comprising:

a clock supply circuit that supplies one or more clocks for driving said one or more functional circuit blocks at a different frequency;

a clock selector circuit that selects a clock being fed to each of the functional circuit blocks for each execution cycle; and

an instruction decoder circuit that feeds a selection signal to the clock selector circuit for selecting a most appropriate clock from one or more clocks by analyzing prescribed bits of an instruction code,

wherein the clock supply circuit and the clock selector circuit are configured so as to change an operating frequency or halt operation of said one or more functional circuit blocks for each execution cycle.

3. A semiconductor integrated circuit having, internally or externally, one or more memory blocks or a single memory block that is dealt with as a plurality of logical memory blocks and executing a set of instructions, comprising:

a clock supply circuit that supplies one or more clocks for driving the semiconductor integrated circuits, a part thereof, said one or more memory blocks, or the single memory block at a different frequency when memory is accessed;

a clock selector circuit that selects a different clock for each execution cycle when memory is accessed; and

a memory select signal circuit that identifies a memory block to be accessed,

wherein the clock supply circuit and the clock selector circuit are configured so as to change an operating frequency or halt operation of the semiconductor integrated circuit, a part thereof, said one or more memory blocks, or the single memory block for each execution cycle in accordance with performance of the memory block that is identified by the memory select signal circuit.

4. A semiconductor integrated circuit having one or more peripheral circuits internally or externally and executing a set of instructions, comprising:

a clock supply circuit that supplies one or more clocks for driving the semiconductor integrated circuits, a part thereof, or said one or more peripheral circuits at a different frequency when said one or more peripheral circuits are accessed;

a clock selector circuit that selects a different clock for each execution cycle when said one or more peripheral circuits are accessed; and

an I/O select signal circuit that identifies a peripheral circuit to be accessed,

wherein the clock supply circuit and the clock selector circuit are configured so as to

change an operating frequency or halt operation of the semiconductor integrated circuit, a part thereof, or said one or more peripheral circuits for each execution cycle in accordance with performance of the peripheral circuit that is identified by the I/O select signal circuit.

5. A semiconductor integrated circuit having one or more memory blocks and a cache memory internally or externally and executing a set of instructions, comprising:

a clock supply circuit that, according to whether a cache hit is experienced or not when data is accessed, supplies one or more clocks for driving the semiconductor integrated circuits, a part thereof, said one or more memory blocks, or the cache memory at a different frequency;

a clock selector circuit that, according to whether a cache hit is experienced or not, selects for each execution cycle a different clock when said one or more memory blocks or the cache memory is accessed; and

a memory select signal circuit that identifies a memory block or the cache memory to be accessed,

wherein the clock supply circuit and the clock selector circuit are configured so as to change an operating frequency or halt operation of the semiconductor integrated circuit, a part thereof, the memory blocks, or the cache memory for each execution cycle according to whether a cache hit is experienced or not when data is accessed.

6. A semiconductor integrated circuit having one or more functional circuit blocks and executing at least either of data processing or instruction processing in a pipeline having a plurality of stages when running a set of instructions, comprising:

a clock supply circuit that supplies one or more clocks for driving the stages at a

different frequency;

a clock selector circuit that selects a different clock to be given to each of the stages for each execution cycle; and

an analyzer circuit that analyzes the instructions and feeds a selection signal to the clock selector circuit for selecting a most appropriate clock for each of the stages from one or more clocks,

wherein the analyzer circuit is arranged so as to analyze the instructions to be executed in each stage of the pipeline and feeds a signal to the clock selector circuit so that, when the stages execute the instructions having a load different from each other, a stage executing an instruction having a lighter load is provided with a slower clock.

7. A semiconductor integrated circuit having one or more functional circuit blocks and executing a set of instructions in a plurality of pipelines configured as a superscalar architecture, comprising:

a clock supply circuit that supplies one or more clocks for driving each of the pipelines at a different frequency;

a clock selector circuit that selects a different clock to be fed to each of the pipelines for each execution cycle;

an analyzer circuit that analyzes the instructions and assign a weight value to each instruction according to an amount of load thereof to be processed; and

an instruction distributor circuit that distributes the instructions among the pipelines by comparing the instructions in a form of the set with weight values contained in a table generated by the analyzer circuit,

wherein the clock selection circuit selects a faster clock for a pipeline that executes an

instruction having a heavier load and selects a slower clock for a pipeline that executes an instruction having a lighter load.

8. A semiconductor integrated circuit having one or more functional circuit blocks and executing a set of instructions in a plurality of processing sections configured as a VLIW (Very Long Instruction Word) architecture, comprising:

a compiler that converts the instructions into a VLIW format and assigns a most suitable clock to each of the instructions in accordance with content thereof to be processed;

a clock supply circuit that supplies one or more clocks for driving each of the processing sections at a different frequency; and

a clock selector circuit that selects the clock assigned to each instruction by the compiler so that the selected clock is fed to a corresponding processing section for each execution cycle,

wherein the semiconductor integrated circuit is configured so as to provide each of the processing sections with an independent clock that enables the processing sections to operate at a frequency different from each other according to a load of the instructions to be executed simultaneously.

9. A semiconductor integrated circuit having one or more functional circuit blocks and executing a set of instructions, comprising:

a clock supply circuit that supplies one or more clocks for driving said one or more functional circuit blocks at a different frequency; and

a clock selector circuit that selects a clock being fed to each of the functional circuit blocks for each execution cycle,

wherein the clock selector circuit has a hierarchically-arranged clock selector architecture in which clock branches are arranged hierarchically in accordance with frequency of use of the clocks in changing an operating frequency or halting operation of each functional circuit block while the instructions are being executed.

10. A semiconductor integrated circuit having one or more functional circuit blocks and executing a set of instructions, comprising:

a compiler that determines a most appropriate clock for each instruction according to content thereof to be executed and writes information thereof thus determined to prescribed bits of a compiled instruction code;

a clock supply circuit that supplies one or more clocks for driving said one or more functional circuit blocks at a different frequency;

a clock selector circuit that selects a clock being fed to each of the functional circuit blocks for each execution cycle; and

an instruction decoder circuit that feeds a selection signal to the clock selector circuit for selecting a most appropriate clock from one or more clocks by analyzing the prescribed bits of the instruction code,

wherein the clock supply circuit and the clock selector circuit are configured so as to change an operating frequency or halt operation of said one or more functional circuit blocks for each execution cycle.